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09/678,733	10/04/2000	Hideyuki Iino	1450.1006	6735

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EXAMINER
DAMIANO, ANNE L

ART UNIT	PAPER NUMBER
2184	4

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/678,733	Applicant(s) IINO ET AL.	
	Examiner Anne L Damiano	Art Unit 2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figures 1, 2 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 2, 4, 6, 7, 10-12 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Mueller (6,226,756).

As in claim 1, Mueller discloses a reset control system for a system having a central processing section (figure 3: component 310) and a peripheral control section which are formed on separate chips (figure 1: components 102, 112 and 114, column 3: lines 9-24) (The system logic, controlling the I/O bus 112, which transfers data to an I/O device or a processor, lines 17-19, is interpreted as a peripheral control section on a separate chip as the central processing section) said reset control system comprising:

A system reset output section for generating and outputting a system reset signal on the basis of an external reset signal (column 7: lines 49-62) (Push-button reset is interpreted as the external reset signal) and an emulator reset signal based on a reset instruction from an emulator for independently implementing a function of said central processing section (column 7: line 63-column 8: line 3 and figure 3),

Wherein the system reset signal output from the system reset output section is supplied to both chips of the central processing section and the peripheral control system (figure 3: components 315, 310, figure 1, components 108, column 7: line 63-column 8: line 3, column 8: line 63-column 9: line 3 and table 3, RSTOUT signal description (column 9: approximately lines 44-46)) (The output of the reset circuit resets the processor and the system logic. Since the system logic controls the I/O devices or peripheral devices, (Figure 1: components 108, 112, 114 and 116) the reset of the system logic is interpreted as being a reset of the peripheral control system.)

As in claims 10 and 16, Mueller discloses a reset control system and method for a system having a central processing section (figure 3: component 310) and a peripheral control section which are formed on separate chips (figure 1: components 102, 112 and 114, column 3: lines 9-24) (The system logic, controlling the I/O bus 112, which transfers data to an I/O device or a processor, lines 17-19, is interpreted as a peripheral control section on a separate chip as the central processing section) said reset control system comprising:

A system reset selection section for selectively outputting, as a system reset signal one of an external reset signal (column 7: lines 49-62) (Push-button reset is interpreted as the external reset signal) and an emulator reset signal based on a reset instruction from an emulator for independently implementing a function of said central processing section (column 7: line 63-column 8: line 3 and figure 3) (Since the system can be restarted by the emulator or a push-button, it is interpreted that some type of selection section for outputting the reset signal exists),

Wherein the system reset signal output from the system reset signal output from the reset selection section is supplied to both chips of the central processing section and the peripheral control system (figure 3: components 315, 310, figure 1, components 108, column 7: line 63-column 8: line 3, column 8: line 63-column 9: line 3, and table 3, RSTOUT signal description (column 9: approximately lines 44-46)) (The output of the reset circuit resets the processor and the system logic. Since the system logic controls the I/O devices or peripheral devices, (Figure 1: components 108, 112, 114 and 116) the reset of the system logic is interpreted as being a reset of the peripheral control system.)

As in claim 2, Mueller discloses the system reset being generated by OR-operating said emulator reset signal and external reset signal (column 8: lines 3-11). (Since the reset circuit is disclosed as possibly being incorporated into a PLD device, which consists of logic gates, it in interpreted as the reset being generated by OR-operating the two reset signals.)

As in claim 4, Mueller discloses the system reset output section being provided in the chip of the central processing section (figure 3: components 315, 370 and 310).

As in claims 6 and 11, Mueller discloses the reset control system further comprising a synchronization processing section for synchronizing activation timing after reset between the central processing section and the peripheral control section, with the synchronization processing section being formed on the chip of the central processing section (figure 4: component 410 and column 11: lines 40-53).

As in claims 7 and 12, Mueller discloses the synchronization processing section comprising an activation enable signal output section for output section for instructing to enable activation after elapse of a predetermined time after reset of the central processing section of the peripheral control section (column 8: lines 58-67, column 10: lines 11-13 and lines 49-65). (The hard reset to system logic, occurring at a certain time, synchronously with the system clock, caused by the RSTOUT signal from the reset circuit, is interpreted as enable activation after elapse of a predetermined time after reset of the central processing section.)

4. Claim 13 is rejected under 35 U.S.C. 102(e) as being anticipated by Satoh (6,415,393).

As in claim 13, Satoh discloses a reset control system for a system having a central processing section, said reset control system comprising a mask processing section for masking an external reset signal when an emulator for independently implementing a function of the central processing section is in operation (column 1: lines 14-20, column 3: lines 44-58, column 8: lines 47-61 and column 9: lines 36-48). (Since the system has the capability of masking an external reset signal, it is interpreted that a mask processing section exists.)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller as applied to claim 1 above.

Regarding claim 3, Mueller discloses the system reset output section being provided in the chip of the central processing section (figure 3: components 315, 370 and 310). However,

Mueller does not specifically disclose the system reset output section being provided in the chip of the peripheral control section.

It would have been obvious to a person skilled in the art at the time the invention was made to put the system reset output section in the chip of the peripheral control section. It would have been obvious because Mueller discloses that his invention is intended to cover various equivalent arrangements within the scope (column 11: lines 60-62). A person skilled in the art would have understood that the system would be essentially the same, had the system reset output section been provided in the chip of the peripheral control section.

7. Claims 5, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller as applied to claim 1 above, and further in view of Satoh (6,415,393).

Regarding claim 5, Mueller discloses the reset control system above. However, Mueller does not specifically disclose a mask processing section. Satoh discloses a mask processing section for masking an external reset signal when the emulator is in operation (column 1: lines 14-20, column 3: lines 44-58, column 8: lines 47-61 and column 9: lines 36-48). (Since the system has the capability of masking an external reset signal, it is interpreted that a mask processing section exists.)

It would have been obvious to a person skilled in the art at the time the invention was made to include the mask processing section taught by Satoh in Mueller's system. It would have been obvious because Satoh's teaches an easily implemented protocol for handling an external

reset when an emulator is in operation. A person skilled in the art would have understood that some type of protocol for handling the external reset and emulator must exist in the system.

As in claim 8, Mueller discloses the reset control system further comprising a synchronization processing section for synchronizing activation timing after reset between the central processing section and the peripheral control section, with the synchronization processing section being formed on the chip of the central processing section (figure 4: component 410 and column 11: lines 40-53).

As in claim 9, Mueller discloses the synchronization processing section comprising an activation enable signal output section for output section for instructing to enable activation after elapse of a predetermined time after reset of the central processing section of the peripheral control section (column 8: lines 58-67, column 10: lines 11-13 and lines 49-65). (The hard reset to system logic, occurring at a certain time, synchronously with the system clock, caused by the RSTOUT signal from the reset circuit, is interpreted as enable activation after elapse of a predetermined time after reset of the central processing section.)

8. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mueller in view of Satoh.

Regarding claim 14, Mueller discloses a reset control method for a system having a central processing section (figure 3: component 310) and a peripheral control section which are

formed on separate chips (figure 1: components 102, 112 and 114, column 3: lines 9-24) (The I/O buses transferring data to an I/O device or a processor, lines17-19, is interpreted as a peripheral control section on a separate chip as the central processing section) said reset control method comprising the steps of:

Generating an external reset signal or an emulator reset signal based on a reset instruction from the emulator (column 7: line 49-column 8: line 3 and figure 3); (Push-button reset is interpreted as the external reset signal.)

And;

Supplying the reset signal to both chips of the central processing section and the peripheral control section (figure 3: components 315, 310, figure 1, components 108, column 7: line 63-column 8: line 3, column 8: line 63-column 9: line 3, and table 3, RSTOUT signal description (column 9: approximately lines 44-46)) (The output of the reset circuit resets the processor and the system logic. Since the system logic controls the I/O devices or peripheral devices, (Figure 1: components 108, 112, 114 and 116) the reset of the system logic is interpreted as being a reset of the peripheral control system.).

However, Mueller does not specifically disclose the step of masking an external reset signal when an emulator for independently implementing a function of the central processing section is in operation (column 1: lines 14-20, column 3: lines 44-58, column 8: lines 47-61 and column 9: lines 36-48).

It would have been obvious to a person skilled in the art at the time the invention was made to include the step of masking the external reset, as taught by Satoh, in Mueller's system. It would have been obvious because Satoh teaches an easily implemented protocol for handling

an external reset when an emulator is in operation. A person skilled in the art would have understood that some type of protocol for handling the external reset while the emulator is in operation must exist in the system.

As in claim 15, Mueller discloses the system reset being generated by OR-operating said emulator reset signal and external reset signal (column 8: lines 3-11). (Since the reset circuit is disclosed as possible being incorporated into a PLD device, which consists of logic gates, it in interpreted as the reset being generated by OR-operating the two reset signals.)

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (703) 305-8010. The examiner can normally be reached on M-F 8:00AM-5:30PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9731. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Anne L Damiano
Examiner
Art Unit 2184

ALD
May 15, 2003

SCOTT BADERMAN
PRIMARY EXAMINER